ABSTRACT OF THE DISCLOSURE

A partitioned source line architecture for reducing leakage and power in a ROM. In one embodiment, a ROM is comprised of a plurality of storage cells organized as an array having M rows and N columns. Each column is associated with a precharged source line that is partitioned into a plurality of source line segments based on the number of row banks of the array. A plurality of local source line decoder circuits corresponding to the row banks are provided for decoding a selected source line segment based on the column address as well as a Bank Select signal generated from the row address of a particular cell. Local pull-down circuitry is provided with each bank for deactivating the selected source line segment upon commencing a memory access operation.